Amendment to the Specification

Please replace Paragraphs [0047] to [0050] at page 8 with the following rewritten paragraphs:

-- **[0047]** Fig. 15 is a diagram ~~of a DLL~~ showing a bias circuit including a positive bias circuit and a negative bias circuit in accordance with an embodiment of the present invention;

[0048] Fig. 16 is a diagram ~~of bias circuits and delay~~ showing the negative bias circuit of Fig. 15;

[0049] Fig. 17 ~~illustrates the current bleeder device of Fig. 16~~ is a diagram showing the positive bias circuit of Fig. 15 and a delay cell; [[and]]

[0050] Fig. 18 ~~illustrates~~ is a diagram showing an implementation of the circuit of Figs. 16 and 17 [[.]];

[0050.1] Fig. 19 is a diagram showing the gate structure of a transistor included in the bias circuit of Fig. 17;

[0050.2] Fig. 20 is a diagram showing a delay lock loop (DLL) with the bias circuit of Fig. 17;

[0050.3] Fig. 21 is a diagram showing a phase lock loop (PLL) with the bias circuit of Fig. 17;

[0050.4] Fig. 22 is a diagram showing a charge pump with the bias circuit of Fig. 17;

[0050.5] Figs. 23a and 23b are diagrams showing an Operational Amplifier with the bias circuit of Fig. 17; and

[0050.6] Fig. 24 is a diagram showing an Input/Output pad with the bias circuit of Fig. 17. --